

multi-layer wiring decal on the support substrate and over the chip. However, this reference differs from the invention.

US 5,106,461 (Volfson et al.) teaches a multi layer interconnect structure of alternating polyimide (dielectric) and metal layers over an IC in a TAB structure.

US 5,635,767 (Wenzel et al.) teaches a method for reducing RC delay by a PBGA that separates multiple metal layers.

US 5,686,764 (Fulcher) shows a flip chip substrate that reduces RC delay by separating the power and I/O traces.

SUMMARY OF THE INVENTION

It is the primary objective of the present invention is to improve the performance of High Performance Integrated Circuits.

Another objective of the present invention is to reduce resistive voltage drop of the power supply lines that connect the IC to surrounding circuitry or circuit components.

Another objective of the present invention is to reduce the RC delay constant of the signal paths of high performance IC's.

Yet another objective of the present invention is to facilitate the application of IC's of reduced size and increased circuit density.

Yet another objective of the present invention is to further facilitate and enhance the application of low resistor conductor metals.

Yet another objective of the present invention is to allow for increased I/O pin count for the use of high performance IC's.

Yet another objective of the present invention is to simplify chip assembly by reducing the need for re-distribution of I/O chip connections.

Yet another objective of the present invention is to facilitate the connection of high-performance IC's to power buses.

Yet another objective of the present invention is to facilitate the connection of high-performance IC's to clock distribution networks.

Yet another objective of the present invention is to reduce IC manufacturing costs by allowing or facilitating the use of less expensive process equipment and by accommodating less strict application of clean room requirements, this as compared to sub-micron manufacturing requirements.

Yet another objective of the present invention is to be a driving force and stimulus for future system-on-chip designs since the present invention allows ready and cost effective interconnection between functional circuits that are positioned at relatively large distances from each other on the chip.

Yet another objective of the present design is to form the basis for a computer based routing tool that automatically routes interconnections that exceed a pre-determined length in accordance with the type of interconnection that needs to be established.

The present invention adds one or more thick layers of dielectric and one or more layers of wide metal lines on top of